REMARKS

Applicants amend the specification and claims 1-7, 10-12, 17-19, 21-24, 27, and 29-31. Claims 34-54 are cancelled without prejudice to their underlying subject matter as being non-elected or the subject of related patent applications.

Since this application is a divisional of allowed application serial number 09/076,728, filed on May 13, 1998, the cited Kurth et al. reference (U.S. Patent Application 09/833,706; Pub. No. 2001/0021122) is not prior art, based on its earliest priority date of July 31, 1998. All rejections over this reference should be withdrawn.

Claims 1-16 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,329,142 (Kitagawa et al.) and U.S. Patent No. 5,776,823 (Agnello et al.). Applicants respectfully traverse this rejection.

Claim 1, as amended, defines a memory cell and recites "two gated vertically stacked bipolar transistors configured to exhibit two bistable current states for storing information, one of said current states being achieved by operation of gate-induced latchup of said transistors." Neither Kitagawa et al. nor Agnello et al., taken individually or in combination, teaches or suggests a device as claimed.

Kitagawa et al. does not teach or suggest a memory device having "two gated vertically stacked bipolar transistors." Nowhere in Kitagawa et al. is disclosed a memory device with a transistor stacked over another transistor. As illustrated in each figure cited in the office action, i.e., figures 2, 6, 7, and 27, and the related text, Kitagawa et al. discloses a row of laterally positioned transistors combined in a self-turn-off semiconductor device, which is never discussed in Kitagawa et al. as being a memory device (the term "memory" is not in Kitagawa et al.). Therefore, Kitagawa et al. does not teach or suggest a vertical device or a memory device as claimed. At least for these reasons Kitagawa et al.'s disclosed semiconductor structure is not that of the claimed device.

Additionally, Kitagawa et al. does not teach or suggest a device for storing information as bistable current states, as recited in the claim. It is not taught or suggested by Kitagawa et al. that its disclosed device can store information.

Additionally, Kitagawa et al. teaches away from the claimed device, making Kitagawa et al. an improper reference for a rejection under 35 U.S.C. § 103(a). Kitagawa et al. instructs that for each embodiment of its disclosed device, its transistors are configured to prevent the device "from being latched up." Column 5, line 68; column 6, lines 19-25; column 9, lines 57-58; and column 21, lines 61-62. Thus, Kitagawa et al. directly teaches away from the recited "operation of gate-induced latchup of said transistors" of claim 1. For this reason alone, the rejection of claims 1-7 should be withdrawn.

Additionally, even if, assuming arguendo, Kitagawa et al. did not teach away from gate induced latch-up, the transistor activation disclosed by Kitagawa et al. does not operate using latch-up, but instead operates on a voltage polarity-based on/off system where a voltage of a positive or negative polarity turns the device on and a voltage of the opposite polarity turns the device off. Column 5, lines 45-60; column 7, lines 27-38; column 9, lines 35-42; column 14, lines 48-56; and column 21, lines 24-34. For this reason as well, Kitagawa et al. does not teach or suggest the elements of the claimed device.

Agnello et al. does not teach or suggest the above-discussed claim elements missing from the disclosure of Kitagawa et al., thus Agnello et al. cannot supplement Kitagawa et al. so as to have rendered the subject matter of claim 1 obvious. More specifically, Agnello et al. does not teach or suggest the recited memory cell or vertically stacked bipolar transistors or a configuration to exhibit two bistable current states or configuration to achieve gate-induced latchup.

Because Kitagawa et al. and Agnello et al. would not have rendered the subject matter of claim 1 obvious and because Kitagawa et al. is an improper reference for an obviousness rejection, independent claim 1 and dependent claims 2-9 are patentable over these references. The 35 U.S.C. § 103(a) rejection of claims 1-9 is respectfully requested to be withdrawn.

Claim 10, as amended, defines a circuit for storing information as one of at least two possible bistable current states and recites "at least one vertical p-n-p-n structure containing a bipolar p-n-p transistor merged with a bipolar n-p-n transistor at central n- and p-regions of said structure" and "a first transistor gate spanning the central n-region of said p-n-p transistor" and "a second transistor gate spanning the central p-region of said n-p-n transistor." Kitagawa et al. and Agnello et al. do not teach or suggest this device as claimed.

As discussed above in relation to claim 1, Kitagawa et al. does not teach any device for storing information, much less one that stores information as one of two possible bistable current states. Additionally, Kitagawa does not teach a "bipolar p-n-p transistor merged with a bipolar n-p-n transistor at central n- and p- regions." Further, Kitagawa et al. does not teach or suggest a first gate spanning the central n-region of a p-n-p transistor and a second gate spanning the central p-region of a n-p-n transistor. For each of these reasons, Kitagawa et al. does not teach or suggest the claimed device. Agnello et al. cannot supplement these deficiencies in the Kitagawa et al. disclosure. None of these claimed features are taught or suggested by Agnello et al., thus these references cannot combine so as to have rendered the subject matter of claim 10 obvious. For these reasons, Applicants respectfully request that the 35 U.S.C. § 103(a) rejection of claims 10-16 be withdrawn.

Claims 17-27 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kitagawa et al. and Agnello et al. Applicants respectfully traverse this rejection.

Claim 17, as amended, defines a SRAM cell and recites "a vertical transistor stack having a first p-region, a first n-region, a second p-region, and a second n-region" and "a first gate bridging said first and second p-regions across the first n-region, and a second gate bridging said first and second n-regions across said second p-region, wherein said first and second gates are configured to produce latch-up in said vertical transistor stack as a current state for storing information in said SRAM cell." Neither Kitagawa et al. nor Agnello et al., taken individually or in combination, teaches or suggests this claimed device.

As discussed above in relation to claim 10, Kitagawa et al. does not teach or suggest a first gate bridging first and second p-regions of a vertical transistor across a first n-region and does not teach or suggest a second gate bridging first and second n-regions of that transistor across a second p-region. As discussed above in relation to claim 1, Kitagawa et al. does not teach or suggest a configuration to produce latch-up in a vertical transistor stack. Additionally, as discussed above in relation to claim 1, Kitagawa et al. does not teach or suggest a memory device, i.e., a device capable of producing "a current state for storing information" as recited by claim 17. Also, as discussed above, Kitagawa et al. teaches away from a device configured to produce latch-up, making Kitagawa et al. an improper reference for an obviousness type rejection. For each of these reasons, claim 17 is patentable over Kitagawa et al. Agnello et al. can supply none of these missing elements of Kitagawa et al. so as to supplement the primary reference to render the subject matter of claim 17 obvious. For these reasons, Applicants respectfully request that the 35 U.S.C. § 103(a) rejection of claims 17-22 be withdrawn.

Claim 23, as amended, defines a SRAM array and recites, in part, "a plurality of vertical transistors, each of said transistors being merged p-n-p and n-p-n transistors" and "a first set of isolation trenches between said vertical transistors for isolating said vertical transistors in a first direction" and "a second set of isolation trenches orthogonal to said first set of trenches for isolating said vertical transistors in a second direction" and "a first gate line in at least some trenches of said first set of isolation trenches, said first gate line

connecting central n-regions of at least some of said vertical transistors" and "a second gate line in at least some of said trenches of said second set of isolation trenches, said second gate line connecting central p-regions of at least some of said vertical transistors." Such a device is not taught or suggested by Kitagawa et al. and Agnello et al.

As discussed above in relation to claim 10, Kitagawa et al. does not teach or suggest vertical transistors that are merged p-n-p and n-p-n transistors. Additionally, Kitagawa et al. does not teach or suggest isolation trenches in two directions, but instead discloses trench electrodes parallel to each other. Additionally, Kitagawa et al. does not teach two gate lines connected to vertical transistors, which connect like p- and n-regions of different transistors. Agnello et al. cannot supplements these deficiencies of the disclosure of Kitagawa et al. so as to have rendered the subject matter of claim 23 obvious. For these reasons, Applicants respectfully request that the 35 U.S.C. § 103(a) rejection of independent claim 23 and depending claims 24-27 be withdawn.

Claims 28-33 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kitagawa et al., Agnello et al., and Kurth et al. Since this rejection relies upon modification of the disclosures of Kitagawa et al. and Agnello et al. with that of Kruth et al., which is not prior art to the pending claims, this rejection is respectfully requested to be withdrawn. Additionally, the above-discussed reasoning relating to the patentability of claims 1-27 over Kitagawa et al. and Agnello et al. provides a basis for the patentability of claims 28-33 as well.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

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Respectfully submitted,

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